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EXAMINER	
SCHECHTER, ANDREW M	
ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 01/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,960	KIM, YONG WAN	
	Examiner	Art Unit	
	Andrew Schechter	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7 and 9-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7 and 9-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/468,354.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/21/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 14 September 2004 have been fully considered but they are not persuasive.

The applicant argues [pp. 5-6] that *Shin '449* and *Taguchi* do not teach the recited feature "a passivation layer ... are formed". The applicant argues that the examiner admits that *Shin '449* does not teach this feature and relies on *Taguchi* to cure this defect. The applicant then argues that *Taguchi's* drain electrode is completely covered by the protection film 51, contrary to the claimed invention (which has a contact hole in the passivation layer (protection film) so that electrical contact is made between the pixel electrode atop the passivation layer and the drain electrode below it). This is not persuasive. What *Shin '449* discloses is "a passivation layer covering the data wire and the thin film transistor, except the drain electrode, the passivation being covered by the pixel electrode"; what *Shin '449* does not disclose is "the passivation layer exposing the gate insulating layer except portions of the gate insulating layer where the data wire, the thin film transistor, and pixel electrodes are formed". The applicant's comment about *Taguchi's* drain electrode being completely covered is therefore totally irrelevant, as *Shin '449* discloses this and *Taguchi* was not relied on for this feature. *Taguchi* was relied on to teach the element not disclosed by *Shin '449.*

Regarding the rejection over *Shin '049* in view of *Taguchi* and *Shin '449*, the applicant makes an analogous argument which is also unpersuasive.

Claim Rejections - 35 USC § 112

2. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 11 recites the limitation "a photoresist pattern covering the data wire and the thin film transistor". It is not clear to the examiner what is meant by this claim.

If the claim means to refer to Fig. 4B, where the photoresist pattern 39 covers the data wire and the TFT, then the claimed device would not satisfy U.S.C. 112, 1st paragraph, since Fig. 4B represents an intermediate product in the processing of making a liquid crystal display, not a liquid crystal display itself (the photoresist layer is removed by step 4C). It seems unlikely that this is the intended meaning.

For examining purposes, it is assumed that "passivation layer" was intended in place of "photoresist pattern", so that it reads "wherein the passivation layer covers the data wire and the thin film transistor". However, in this case, the claim does not further limit the scope of the independent claim 7, which already recites "a passivation layer covering the data wire and the thin film transistor".

Claim Objections

3. Claim 12 is objected to because of the following informalities: "passviation" in line 9 should be "passivation". Appropriate correction is required.

4. Claim 11 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

As discussed above, claim 11 does not further limit the previous claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7 and 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Shin,* U.S. Patent No. 5,825,449 in view of *Taguchi,* U.S. Patent No. 5,963,279.

Shin '449 discloses [see Fig. 2, for instance] a liquid crystal display comprising:

a substrate [1];

a gate wire on the substrate including a gate electrode [the portion of 2 under the TFT] and a gate line [the portion of 2 connecting from the TFT to the gate pad 2C, required in order to apply a voltage to the TFT, see col. 3, lines 44-49; not shown in Fig. 2, it is 600 in Fig. 6];

a gate insulating layer [3] covering an exposed surface of the substrate including the gate wire;

a thin film transistor formed in an active layer [4] on the gate insulating layer, having the gate electrode [2] and further having a source electrode [7] and a drain electrode [8];

a data wire on the gate insulating layer including a data line [the "source wiring" leading from the transistor to 7A, see col. 4, lines 1-5], the source electrode, and the drain electrode [col. 3, line 63 – col. 4, line 5];

a pixel electrode [6] connected to the drain electrode of the thin film transistor;

a passivation layer [9] covering the data wire and the thin film transistor, except the drain electrode [see Fig. 2], being covered by the pixel electrode [see Fig. 2];

a data pad [2A, 7A] at an end of the data line, being covered with the passivation layer;

a contact hole in the passivation layer exposing an exposed portion of the data pad [see Fig. 2];

a data pad covering layer [6A] covering the exposed portion of the data pad [see Fig. 2].

Shin '449 does not disclose the passivation layer exposing the gate insulating layer except portions of the gate insulating layer where the data wire, thin film transistor, and pixel electrode are formed. *Taguchi* discloses [see Figs. 10-19] a method of preventing defects in an analogous liquid crystal display which, when applied to the device of *Shin '449*, causes the passivation layer to expose the gate insulating layer except portions where the data wire, thin film transistor, and pixel electrode are formed.

Taguchi's method of preventing defects [see Figs. 9-19] aims to prevent defects caused by a pixel electrode short-circuiting to neighboring electrodes, by etching around the border of the pixel electrode [see Fig. 9] using the gate insulating layer as an etch-stop [see Fig. 19]. (*Taguchi* does not anticipate the claimed invention, because the pixel electrode in *Taguchi* is not above a passivation layer, as it is in *Shin '449*.) Applying this method of preventing defects to the device of *Shin '449*, one of ordinary skill in the art would etch around the border of the pixel electrode using the gate insulating layer as an etch-stop, with the result that *Shin '449's* passivation layer would expose the gate insulating layer, except portions where the data wire, thin film transistor, and pixel electrode are formed.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use *Taguchi's* method of preventing defects in the device of *Shin '449*, motivated by *Taguchi's* teaching that by thus eliminating short-circuits between the electrodes, "display defects are drastically reduced, display quality is improved and production yield is also improved" [abstract]. Claim 7 is therefore unpatentable.

Shin '449 also discloses the passivation layer covering the data wire and thin film transistor, and exposing a portion of the pixel electrode [see Fig. 2], so claim 10 is also unpatentable.

As discussed above, claim 11 is assumed to recite the passivation layer covering the data wire and TFT, which is disclosed by *Shin '449*. Claim 11 is therefore unpatentable.

Considering claim 16, claim 16 recites the limitations of claim 7 discussed above, and adds the limitation that the passivation layer at the portion where a pattern defect is disposed is removed. As discussed above, the point of *Taguchi's* removal of the passivation layer is remove such pattern defects [53a-e], so claim 16 is also unpatentable.

Considering the additional limitations of claim 12 over those of claim 7 already considered, claim 12 recites a pattern defect on the gate insulating layer, wherein the pattern defect is opened by removing partially the passivation layer. As discussed above, the point of *Taguchi's* removal of the passivation layer, using the gate insulating layer as an etch-stop, is to remove such pattern defects [53a-e], which are on the gate insulating layer. Claim 12 is therefore unpatentable.

The gate insulating layer except portions of the gate insulating layer where the data wire, TFT, and pixel electrode are formed are exposed (as discussed for claim 7), so claim 13 is also unpatentable.

Taguchi discloses that a pattern defect [53d, for instance] is generated from residue of a substance used to form the data wire (insofar as the pattern defect consists of a residue of the substance used to form the data wire), so claim 15 is also unpatentable.

Taguchi discloses more generally that the cause of such pattern defects is dust particles [66, for instance] which act as undesired etch-masks [col. 6, lines 25-33]. *Taguchi* does not explicitly disclose that the dust can be a residue of a substance used to form an active layer of the TFT. However, this is essentially a product-by-process

limitation (reciting that the step of generating the pattern defect uses the residue of a substance used to form the active layer); such claims are only limited to the structure implied by the steps, not the manipulations of the recited steps [see MPEP 2113]. Here, the structures appear to be substantially identical (both have active layers formed, then pattern defects formed, then the pattern defects are removed); there appear to be no distinctive characteristics given to the structure to distinguish between the cases where the active layer residue did or did not generate the pattern defect. In such cases the burden shifts to the applicant to show that there is an unobvious difference [see MPEP 2113]. Claim 14 is therefore unpatentable.

7. Claims 7 and 9-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Shin et al.,* U.S. Patent No. 5,737,049 in view of *Taguchi,* U.S. Patent No. 5,963,279 and further in view of *Shin,* U.S. Patent No. 5,825,449.

Shin '049 discloses [see Figs. 2, 3, and 5, for instance] a liquid crystal display comprising:

a substrate [1];

a gate wire on the substrate including a gate electrode [21] and a gate line [40];

a gate insulating layer [24, or 23 and 24] covering an exposed surface of the substrate including the gate wire;

a thin film transistor formed in an active layer [25] on the gate insulating layer, having the gate electrode [21] and further having a source electrode [29] and a drain electrode [30];

a data wire on the gate insulating layer including a data line [50], the source electrode, and the drain electrode [col. 5, lines 25-27 and col. 6, lines 59-60];

a pixel electrode [33] connected to the drain electrode of the thin film transistor;

a passivation layer [31] covering the data wire and the thin film transistor, except the drain electrode [see Fig. 2], being covered by the pixel electrode [see Fig. 2].

Shin '049 does not disclose the passivation layer exposing the gate insulating layer except portions of the gate insulating layer where the data wire, thin film transistor, and pixel electrode are formed. *Taguchi* discloses [see Figs. 10-19] a method of preventing defects in an analogous liquid crystal display which, when applied to the device of *Shin '049*, causes the passivation layer to expose the gate insulating layer except portions where the data wire, thin film transistor, and pixel electrode are formed.

Taguchi's method of preventing defects [see Figs. 9-19] aims to prevent defects caused by a pixel electrode short-circuiting to neighboring electrodes, by etching around the border of the pixel electrode [see Fig. 9] using the gate insulating layer as an etch-stop [see Fig. 19]. (*Taguchi* does not anticipate the claimed invention, because the pixel electrode in *Taguchi* is not above a passivation layer, as it is in *Shin '049*.) Applying this method of preventing defects to the device of *Shin '049*, one of ordinary skill in the art would etch around the border of the pixel electrode using the gate insulating layer as an etch-stop, with the result that *Shin '049's* passivation layer would expose the gate insulating layer, except portions where the data wire, thin film transistor, and pixel electrode are formed.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use *Taguchi's* method of preventing defects in the device of *Shin '049*, motivated by *Taguchi's* teaching that by thus eliminating short-circuits between the electrodes, "display defects are drastically reduced, display quality is improved and production yield is also improved" [abstract].

Shin '049 also does not disclose the data pad, contact hole, and data pad covering layer recited by claim 7. *Shin '049* is silent on the subject of such data pads. *Shin '449*, however, does disclose a data pad [2A, 7A] at an end of the data line, being covered with the passivation layer, a contact hole in the passivation layer exposing an exposed portion of the data pad [see Fig. 2], and a data pad covering layer [6A] covering the exposed portion of the data pad [see Fig. 2]. It would have been obvious to one of ordinary skill in the art at the time of the invention to use these data pads in the device of *Shin '049*, motivated by *Shin '449*'s teaching that this data pad structure "does not require the step of exposing the pad directing after depositing the gate insulating film, and the source and gate pads are exposed by etching during the passivation process" [col. 4, lines 35-39], thereby saving manufacturing steps, and "the problem of high contact resistance between the source pad and the source, caused by forming the source pad from the gate material, can be avoided" [col. 4, lines 43-46], so the quality of the electrical connections using this data pad structure is high.

Claim 7 is therefore unpatentable.

Shin '049 also discloses [see Fig. 5] a part of the data wire on the gate insulating layer over the gate line comprises a subsidiary electrode [52], wherein the subsidiary

electrode comprises an exposed portion [the portion below the contact hole] which is connected to the pixel electrode [33] and a remainder portion being covered with the passivation layer [the portion around the edge of the contact hole]. Claim 9 is therefore unpatentable as well.

Shin '049 also discloses the passivation layer covering the data wire and thin film transistor, and exposing a portion of the pixel electrode [see Fig. 2], so claim 10 is also unpatentable.

As discussed above, claim 11 is assumed to recite the passivation layer covering the data wire and TFT, which is disclosed by *Shin '449*. Claim 11 is therefore unpatentable.

Considering claim 16, claim 16 recites the limitations of claim 7 discussed above, and adds the limitation that the passivation layer at the portion where a pattern defect is disposed is removed. As discussed above, the point of *Taguchi's* removal of the passivation layer is remove such pattern defects [53a-e], so claim 16 is also unpatentable.

Considering the additional limitations of claim 12 over those of claim 7 already considered, claim 12 recites a pattern defect on the gate insulating layer, wherein the pattern defect is opened by removing partially the passivation layer. As discussed above, the point of *Taguchi's* removal of the passivation layer, using the gate insulating layer as an etch-stop, is to remove such pattern defects [53a-e], which are on the gate insulating layer. Claim 12 is therefore unpatentable.

The gate insulating layer except portions of the gate insulating layer where the data wire, TFT, and pixel electrode are formed are exposed (as discussed for claim 7), so claim 13 is also unpatentable.

Taguchi discloses that a pattern defect [53d, for instance] is generated from residue of a substance used to form the data wire (insofar as the pattern defect consists of a residue of the substance used to form the data wire), so claim 15 is also unpatentable.

Taguchi discloses more generally that the cause of such pattern defects is dust particles [66, for instance] which act as undesired etch-masks [col. 6, lines 25-33]. *Taguchi* does not explicitly disclose that the dust can be a residue of a substance used to form an active layer of the TFT. However, this is essentially a product-by-process limitation (reciting that the step of generating the pattern defect uses the residue of a substance used to form the active layer); such claims are only limited to the structure implied by the steps, not the manipulations of the recited steps [see MPEP 2113]. Here, the structures appear to be substantially identical (both have active layers formed, then pattern defects formed, then the pattern defects are removed); there appear to be no distinctive characteristics given to the structure to distinguish between the cases where the active layer residue did or did not generate the pattern defect. In such cases the burden shifts to the applicant to show that there is an unobvious difference [see MPEP 2113]. Claim 14 is therefore unpatentable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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18 January 2005